Amendments to the Claims:

The listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Currently Amended) A semiconductor device having a self-aligned contact, the semiconductor device comprising:

a plurality of conductive patterns formed to be adjacent to one another by sequentially stacking and patterning a first conductive layer and a mask layer on a particular underlying layer;

a first insulation layer filling a gap between adjacent conductive patterns, the first insulation layer being formed of a first insulating material and being formed laterally adjacent to and not underneath the conductive patterns;

a second insulation layer having a spacer shape, the second insulation layer formed at the sides of each conductive pattern and over the first insulation layer, the second insulation layer being formed of a second insulating material different from the first insulating material; and

a second conductive layer, the second conductive layer being a single uninterrupted layer formed over the conductive patterns and having a contact portion that fills ~~filling~~ a contact hole which is self-aligned with respect to the second insulation layer between adjacent conductive patterns, the contact hole passing through the first insulation layer, the first insulation layer extending between adjacent conductive patterns, and between the contact portion of the second conductive layer and the conductive patterns, and having a single aligned planar top surface throughout the distance between at least one of the conductive patterns and the contact portion of the second conductive layer.

2. (Currently Amended) The semiconductor device of claim 1, wherein the top surface of the first insulation layer is lower than the top surface of the first conductive layer of each conductive ~~layer~~ pattern.

3. (Currently Amended) The semiconductor device of claim 1, wherein the top surface of the first insulation layer is higher than the top surface of the first conductive layer of each conductive ~~layer~~ pattern.

4. (Original) The semiconductor device of claim 1, wherein an etching rate of the first insulation layer is larger than that of the second insulation layer.

5. (Original) The semiconductor device of claim 1, wherein the dielectric constant of the first insulation layer is smaller than that of the second insulation layer.

6. (Original) The semiconductor device of claim 1, wherein the first insulation layer is formed of a silicon oxide layer.

7. (Original) The semiconductor device of claim 1, wherein the second insulation layer is formed of a silicon nitride layer.

8.-13. (Canceled)

14. (Currently Amended) The semiconductor device of claim 1, wherein the first conductive layer of each conductive ~~layer~~ pattern is a bit line, and the second conductive layer serves to connect a storage electrode of a semiconductor capacitor to a semiconductor substrate.

15. (Currently Amended) The semiconductor device of claim 1, wherein the first conductive layer of each conductive ~~layer~~ pattern is a gate electrode, and the contact contacts the surface of a semiconductor substrate.

16. (Withdrawn) A method for fabricating a semiconductor device having a self-aligned contact, the method comprising:

forming a plurality of conductive layer patterns adjacent to one another by sequentially stacking a first conductive layer and a mask layer on a particular underlying layer and patterning the first conductive layer and the mask layer;

filling a gap between adjacent conductive layer patterns by depositing a first insulation layer on the surface of the underlying layer on which the conductive layer patterns are formed;

etching the entire surface of the first insulation layer to expose the upper portion of each conductive layer pattern;

forming a spacer of a second insulation layer on the sides of each exposed conductive layer pattern;

forming a contact hole self-aligned with respect to spacers so that the surface of the underlying layer between adjacent conductive layer patterns is exposed; and

forming a second conductive layer by filling the contact hole with a conductive material.

17. (Withdrawn) The method of claim 16, further comprising planarizing the surface of the first insulation layer after filling the gap between the adjacent conductive layer patterns with the first insulation layer.

18. (Withdrawn) The method of claim 16, further comprising forming an interlayer insulation layer, the surface of which is planarized, on the entire surface of the resultant structure obtained after forming the spacer of the second insulation layer.

19. (Withdrawn) The method of claim 16, further comprising forming an insulation layer used as an etching stopper on the entire surface of the resultant structure obtained after forming the conductive layer patterns.

20. (Withdrawn) The method of claim 19, further comprising forming a spacer of the insulation layer used as the etching stopper on the sides of each conductive layer pattern by etching the insulation layer used as the etching.

21. (Currently Amended) A semiconductor device having a self-aligned contact, the semiconductor device comprising:

a plurality of conductive patterns formed to be adjacent to one another by sequentially stacking and patterning a first conductive layer and a mask layer on a particular underlying layer;

a first insulation layer filling a gap between adjacent conductive patterns, the first insulation layer being formed of a first insulating material and being formed laterally adjacent to and not underneath the conductive patterns;

a second insulation layer having a spacer shape, the second insulation layer formed at the sides of each conductive pattern and over the first insulation layer, the second insulation layer being formed of a second insulating material different from the first insulating material;

a second conductive layer, the second conductive layer being a single uninterrupted layer formed over the conductive patterns and having a contact portion that fills ~~filling~~ a contact hole which is self-aligned with respect to the second insulation layer between adjacent conductive patterns, the contact hole passing through the first insulation layer, the first insulation layer extending between adjacent conductive patterns, and between the contact portion of the second conductive layer and the conductive patterns, and having a single aligned planar top surface between at least one of the conductive patterns and the contact portion of the second conductive layer; and

a third insulation layer provided between the first insulation layer and the sides of each conductive layer pattern and between the second insulation layer and the side of the conductive layer pattern.

22. (Previously Presented) The semiconductor device of claim 21, wherein the third insulation layer is formed of a silicon nitride layer to a thickness of 50-200 Å.

23. (Currently Amended) The semiconductor device of claim 21, wherein the top surface of the first insulation layer is lower than the top surface of the first conductive layer of each conductive ~~layer~~ pattern.

24. (Currently Amended) The semiconductor device of claim 21, wherein the top surface of the first insulation layer is higher than the top surface of the first conductive layer of each conductive ~~layer~~ pattern.

25. (Previously Presented) The semiconductor device of claim 21, wherein an etching rate of the first insulation layer is larger than that of the second insulation layer.

26. (Previously Presented) The semiconductor device of claim 21, wherein the dielectric constant of the first insulation layer is smaller than that of the second insulation layer.

27. (Previously Presented) The semiconductor device of claim 21, wherein the first insulation layer is formed of a silicon oxide layer.

28. (Previously Presented) The semiconductor device of claim 21, wherein the second insulation layer is formed of a silicon nitride layer.

29. (Currently Amended) The semiconductor device of claim 21, wherein the first conductive layer of each conductive ~~layer~~ pattern is a bit line, and the second conductive layer serves to connect a storage electrode of a semiconductor capacitor to a semiconductor substrate.

30. (Currently Amended) The semiconductor device of claim 21, wherein the first conductive layer of each conductive ~~layer~~ pattern is a gate electrode, and the contact contacts the surface of a semiconductor substrate.

31. (Currently Amended) A semiconductor device having a self-aligned contact, the semiconductor device comprising:

a plurality of conductive patterns formed to be adjacent to one another by sequentially stacking and patterning a first conductive layer and a mask layer on a particular underlying layer;

a first insulation layer filling a gap between adjacent conductive patterns, the first insulation layer being formed of a first insulating material and being formed laterally adjacent to and not underneath the conductive patterns;

a second insulation layer having a spacer shape, the second insulation layer formed at the sides of each conductive pattern and over the first insulation layer, the second insulation layer being formed of a second insulating material different from the first insulating material;

a second conductive layer, the second conductive layer being a single uninterrupted layer formed over the conductive patterns and having a contact portion that fills ~~filling~~ a contact hole which is self-aligned with respect to the second insulation layer between adjacent conductive patterns, the contact hole passing through the first insulation layer, the first insulation layer extending between adjacent conductive patterns, and between the contact portion of the second conductive layer and the conductive patterns, and having a single aligned planar top surface between at least one of the conductive patterns and the contact portion of the second conductive layer; and

a third insulation layer provided on the surfaces of the conductive patterns and on the surface of the underlying layer, the third insulating layer being absent from ~~except for~~ a portion ~~contacting~~ of the underlying layer that contacts the second conductive layer ~~and on the surfaces of the conductive layer patterns~~.

32. (Previously Presented) The semiconductor device of claim 31, wherein the third insulation layer is formed of a silicon nitride layer to a thickness of 50-200 Å.

33. (Currently Amended) The semiconductor device of claim 31, wherein the top surface of the first insulation layer is lower than the top surface of the first conductive layer of each conductive ~~layer~~ pattern.

34. (Currently Amended) The semiconductor device of claim 31, wherein the top surface of the first insulation layer is higher than the top surface of the first conductive layer of each conductive ~~layer~~ pattern.

35. (Previously Presented) The semiconductor device of claim 31, wherein an etching rate of the first insulation layer is larger than that of the second insulation layer.

36. (Previously Presented) The semiconductor device of claim 31, wherein the dielectric constant of the first insulation layer is smaller than that of the second insulation layer.

37. (Previously Presented) The semiconductor device of claim 31, wherein the first insulation layer is formed of a silicon oxide layer.

38. (Previously Presented) The semiconductor device of claim 31, wherein the second insulation layer is formed of a silicon nitride layer.

39. (Currently Amended) The semiconductor device of claim 31, wherein the first conductive layer of each conductive ~~layer~~ pattern is a bit line, and the second conductive layer serves to connect a storage electrode of a semiconductor capacitor to a semiconductor substrate.

40. (Currently Amended) The semiconductor device of claim 31, wherein the first conductive layer of each conductive ~~layer~~ pattern is a gate electrode, and the contact contacts the surface of a semiconductor substrate.